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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Lee et al. Attorney Docket No.: ALTRP194

Patent: 7,061,268 B1 Issued: June 13, 2006

Title: INITIALIZING A CARRY CHAIN IN A PROGRAMMABLE LOGIC DEVICE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on April 23, 2007 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

CLAIMS:

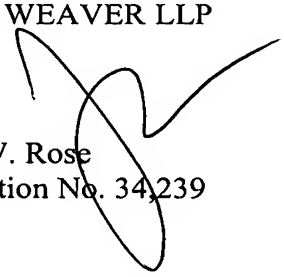
1. In line 2 of claim 14 (column 13, line 16) change "initiation" to --initialization--. This appears correctly in Amendment B as filed on December 23, 2005, on page 5, paragraph 3, line 2, as claim 15.

2. In line 14 of claim 21 (column 14, line 12) delete "and". This appears correctly in Amendment B as filed on December 23, 2005, on page 7, paragraph 3, line 9, as claim 24.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. ALTRP194).

Respectfully submitted,
BEYER WEAVER LLP



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a first logic gate connected to a first input of the multiplexer,

a second logic gate connected to second input of the multiplexer, and

wherein the first and second logic gates are connected to an initialization signal.

13. (Cancelled)

14. (Original) The logic circuit of claim 12,

wherein the adder includes:

a non-inverted carry input signal,

an inverted carry out signal,

a first multiplexer that generates the inverted carry out signal,

and a second multiplexer that generates a sum; and

wherein the initialization circuit includes;

a third multiplexer with an output connected to a first input of the first multiplexer and an input connected to a second input of the first multiplexer,

a logic gate connected to the second multiplexer, and

wherein the third multiplexer and the logic gate are connected to an initialization signal.

15. (Original) The logic circuit of claim 12, further comprising;

a initialization value selection circuit connected to the initialization circuit, wherein the initialization value selection circuit is configured to allow selection of an initialization value for the initialization circuit.

16. (Original) The logic circuit of claim 15, wherein the initialization value can be set to a high or low value.

22. (Currently Amended) A programmable logic device comprising:

an array of logic elements grouped into a plurality of logic blocks;

a first series of logic elements disposed within a logic block, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;

a carry chain connecting the first series of logic element;

an initialization circuit connected to the carry chain to initialize the carry chain;

a first path connecting the first series of logic elements; ~~and~~

a second path connecting a second series of logic elements,

wherein the logic elements in the first series are a subset of the logic elements in the second series**; and**

a logic circuit connected to the initialization circuit.

23. (Original) The programmable logic device of claim 22, wherein the initialization circuit comprises:

a first initialization circuit connected to the first path; and

a second initialization circuit connected to the second path.

24. (Currently Amended) A programmable logic device comprising:

an array of logic elements grouped into a plurality of logic blocks;

a first series of logic elements disposed within a logic block, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;

a carry chain connecting the first series of logic elements;

an initialization circuit connected to the carry chain to initialize the carry chain;

an initialization value selection circuit connected to the initialization circuit, wherein the initialization value selection circuit is configured to selection of an initialization value for the initialization circuit, ~~and~~ wherein the initialization value can be set to a high or low value**; and**

a logic circuit connected to the initialization circuit.

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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,061,268 B1 Page 1 of 1

DATED : June 13, 2006

INVENTOR(S) : Lee et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Claims:

In line 2 of claim 14 (column 13, line 16) change "initiation" to --initialization--.

In line 14 of claim 21 (column 14, line 12) delete "and".

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